**Submission Instruction**

### (5 points will be deducted if you do not follow this instruction)

### There are in total 3 folders to submit: part1, part2, and part3.

### Part 1: Basic Alarm Clock

### All the required files should be placed in a folder called “part1”. NO other files(.wlf, .qpf, etc..) are allowed, points will be deducted if you submit other files.

* Verilog source files (.sv files only), and a Verilog source testbench (.sv file only) required ONLY for Part1 to function.
* A screenshot (name the file as “RTL.png”) of the RTL viewer top level schematic/block diagram in Quartus
* A screenshot (name the file as “transcript.png”) of the Modelsim transcript, showing correct alarm functionality
* A report file (name the file as “report.pdf” or “report.txt”) explaining how you tested your alarm clock

### Part 2: Days of the Week

### All the required files should be placed in a folder called “part2”. NO other files(.wlf, .qpf, etc..) are allowed, points will be deducted if you submit other files.

* The format of the display Day of week/Hour/Min.

For example:"01234" means it is Monday(0) at 12:34.

* A set of all necessary Verilog files(.sv files only) separate from the files for Part 1.

For example, if your Part 1 has files “A.sv” and “B.sv”, in Part 2 you modified “A.sv” and added a “C.sv”. Then only put your modified “A.sv” (do not change its filename) and the new “C.sv” in the folder “part2”.

* Or, you can choose to submit **all** necessary Verilog files(.sv files only) for part2, no matter if it already exists in part1 folder and unmodified or not.
* An expanded testbench (still name it as lab2\_tb.sv) that covers and checks the day of the week functionality

Passing the lab2\_tb.sv testbench should tell us your design should function correctly for both part1 and part2.

* A screenshot (name the file as “RTL.png”) of the RTL viewer top level schematic/block diagram in Quartus
* A screenshot (name the file as “transcript.png”) of the ModelSim transcript showing correct day of the week functionality
* A report file (name the file as “report.pdf” or “report.txt”) explaining day of the week enhancement

### Part 3: Date and Month

### All the required files should be placed in a folder called “part3”. NO other files(.wlf, .qpf, etc..) are allowed, points will be deducted if you submit other files.

* The format of the display Month/Date/Day of week/Hour/Min.

For example: "050601234" should be interpreted as"05-06-0-12-34", which means: May(05) 6th, it is Monday(0), at 12:34.

Please note **the Date/Month should start from "1".** That is, 1 means Jan, 2 means Feb, 12 means Dec.

* [important] All necessary Verilog files (.sv files only) required for Part 3 (you should include all the files the Part 3 needs to function without I manually copy any files from part1 or part2 over)

For example, part1 has file A.sv and B.sv, part2 has a modified A.sv and a new C.sv; in part3 you modified C.sv and added D.sv; then besides the modified C.sv and the new D.sv, you still need to include the latest A.sv in part2, and the B.sv in part1.

* An expanded testbench (still name it as lab2\_tb.sv) that covers and checks the day of the week functionality

Passing this lab2\_tb.sv testbench should tell us your design should function correctly for all part1, part2, and part3.

* A screenshot (still name the file as “RTL.png”) of the RTL viewer top level schematic/block diagram in Quartus
* A screenshot (still name the file as “transcript.png”) of the ModelSim transcript showing correct functionality

Sample submission structure:

 